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# 64 BIT RIPPLE CARRY ADDERUSING BOOSTED CMOS DIFFERENTIAL LOGIC

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## ABSTRACT

This paper features boosted CMOS differential logic which has high speed used in ripple carry adders. The proposed logic style gives improved switching speed by boosting the gate–source voltage of transistors with timing-critical signal paths. The logic circuit also reduces area by allowing a single boosting circuit shared by complementary outputs. Logic gates were implemented in a 0.18-µm process of CMOS whose comparison results shows that the energy delay product of the suggested logic style improved by 50% as compared to conventional logic circuits at 1.8 supply voltage. The experimental result for 64 bit ripple carry adder using the proposed logic style indicated that the addition time is minimizes as compared to conventional CMOS circuits.

***Keywords****: Addition time, Voltage boosting, Adder, Energy delay, Voltage scaling*

## I. INTRODUCTION

Bootstrapping is an effective method for speed development and reduction of power. One of the famous methodologies of reduction of power consumed by CMOS digital circuit is scaling down of supply voltage. This is due to the switching power consumption of the circuit which has quadratic relationship on supply voltage. In certain cases the circuit to be carried in the sub threshold region to obtain maximum energy efficiency. However this method is restricted to used in a low-end design where the speed is secondary concern.. To design a medium and high end in which speed performance and energy efficiency are important much aggressive voltage scaling is not necessary and therefore a close-threshold voltage design is more accurate for obtaining high energy efficiency without severe speed degradation. When the supply voltage scaling near the threshold voltage the speed performance of conventional CMOS circuits like static CMOS logic, the differential cascade voltage switch (DCVS) logic and the domino logic is less required due to the reduction in overdrive voltage (VGS − VTH) of transistors. To eliminate this problem a bootstrapped CMOS large capacitive-load driver was suggested. It was alternative to the speed degradation problem. It gives better the switching speed at low supply voltage using the voltage of some internally nodes to be boosted. For operation of fast logic at low supply voltage CMOS bootstrapped dynamic logic (BDL) was suggested. However, the speed of this logic circuit was not good enough due to the latency bootstrapping bulky circuit which was superimposed on the full latency of the circuit. To eliminate the above problems and to improve the switching activities boosting CMOS differential logic circuit is suggested in this paper. It reduces the area and also eliminates the problem of inefficiency. And the latency issues can resolve by the block of voltage boosting given directly to the differential logic tree.

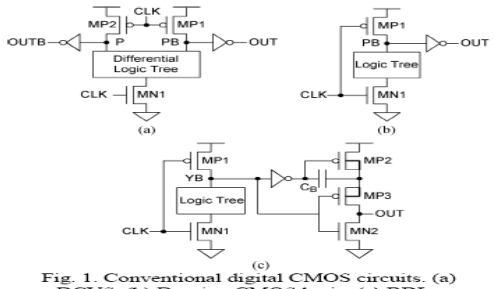


Fig. 1. Conventional digital CMOS circuits. (a) DCVS. (b) Domino CMOS logic. (c) BDL.

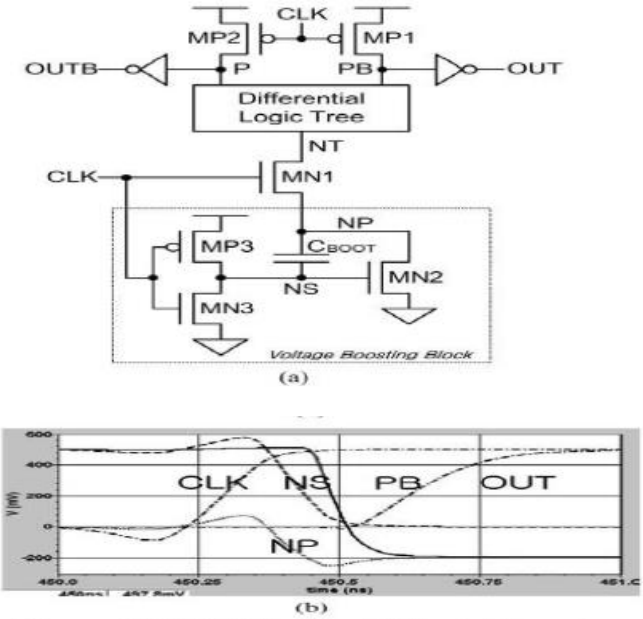


Fig.2 Proposed BCDL. (a) Structure. (b) Simulated waveforms.

***Fig. (a) shows a generic structure of the proposed logic style i.e. boosted CMOS***

It contains a differential logic block known as precharged and a block of voltage- boosting. The voltage-boosting block is shown in the box of dotted line at the lower part of the circuit, is made of transistors like MN2, MN3, and MP3 and CBOOT known as boosting capacitor and it is used to boost the voltage of NP below the ground. The logic block of precharged differential which is contains a differential logic tree with transistor MN1, precharge transistors known as MP1 and MP2, and output inverters get the boosted voltage at NP and calculate the output logic values. It has operation in two phases first is a precharge phase and second is a boosted evaluation phase. The circuit when in the precharge phase then CLK is low. During the precharge phase, the precharged differential logic block is isolated from the voltage-boosting block since MN1 is off. Precharge nodes known as P and PB which are in the differential logic block are precharged by MP1 and MP2 to the supply voltage resulting outputs OUT and OUTB identically low. During same time transistors like MP3 and MN2 which are in block of the voltage- boosting turn on, giving NS and NP to high and low respectively. A voltage similar to the supply voltage is then applied across CBOOT. When CLK goes to high, the circuit changes into the phase of boosted evaluation. When CLK changes to high transistor MN1 is on and the differential logic tree is connected to the voltage boosting block. During same time transistor NS is pulled down approaches the ground giving transistor NP and NT boosted below the ground with the help of capacitive coupling by CBOOT. At the same time the gate source voltages of transistor MN1 and transistors which are in the logic tree are enhanced producing the increase in driving strength of the mentioned transistors. However a little forward source body voltage included in these transistors through voltage of boosting source below the ground resulting in threshold voltage reduction of these transistors, increasing the driving strength of these transistors. The boosted voltage available at NT is then goes to P or PB by the logic tree which depends on input data. At the same time the gate–source voltage of the pmos transistor known as driver transistor is also increasing result in enhancement of driving strength. All these increasing driving strength effects with the help of boosting are combined together with the timing-critical signal paths that is from inputs to the outputs from precharge nodes showing a improvement in switching speed at a region of low- voltage. The BCDL simulated waveforms of this phase are given in Fig. 2(b) in which a supply voltage of 0.5 voltage is used. When CLK reaches high transistor MN1 is on and the differential logic tree is connected to the voltage boosting block. During same time ns ispulled down reaches to ground and with the help of capacitive coupling by CBOOT resulting NP and NT which is boosted below the ground. As indicated in Fig. 2(b) NP reaches to -250 mV andit settles near to -200 mV by action of boosting. At this time the gate source voltages of transistors MN1 and transistors which are on the logic tree are

enhanced that resulting in an increase in driving strength of these transistors. However a small forward source-body voltage included in these transistors through voltages of boosting source below the ground resulting in a a reduction of threshold voltages of these transistors and increasing their driving strength. However, the boosted voltage available at NT is then goes to P or PB by the logic tree depends on input data in Fig. 2(b) input data are in such a way that PB is pulled down that is below the ground. The gate-source voltage of pmos driver transistor is also enlarged and this enhances is driving strength. Along the timing-critical signal paths from the inputs to the outputs from precharge nodes all these driving strength increasing effects through boosting are combined together showing improvement in switching speed at a region of low-voltage.

## II. SIMULATION COMPARISION

A ripple carry chain of 8 bit was used in the BCDL adder to give boosting operation foreach stage of carry chain whereas Manchester carry chain of 8 bit was used in the earlier DCVS and BDL adders for propagation of high speed carry. Fig.3 indicates the previous structure of an 8 bit ripple carry chain used in the BCDL adders.

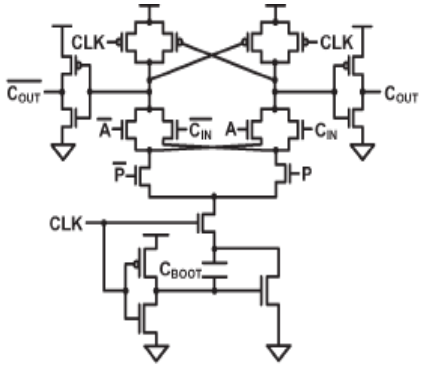


***Fig.3. conventional structure of 8 bit ripple carry chain used in BCDL***

Propagation of carry is carried out by XOR gate when both input remains 1 whereas its generation is performed when either of its input are equal to 1. Fig.4 indicates the structure of XOR gate for propagation of carry.

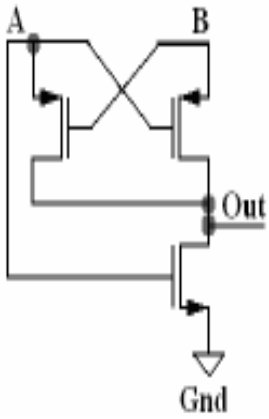


***Fig. 4. XOR gate***

Table 1 gives the total delay, power consumption and power delay product of suggested 1 bit ripple carry adder when compared with previous 1 bit ripple carry adder.

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| Ripple Carry Adder | Rising delay(*) | Falling Delay(*) | Total delay(*) | Power consumption(*) | PDP (&) |
|---|---|---|---|---|---|
| 22T (Prop.) | .39 | .088 | 19.54 | 16 | 313 |
| 24T | .39 | .22 | 19.61 | 16 | 314 |
| Units- *=ns, &=ns x ns | | | | | |

***Table 1- 1 bit ripple carry adder***

Fig.5 gives the rising delay, propagation delay, power consumption and power delay product chart of 1 bit ripple carry adder

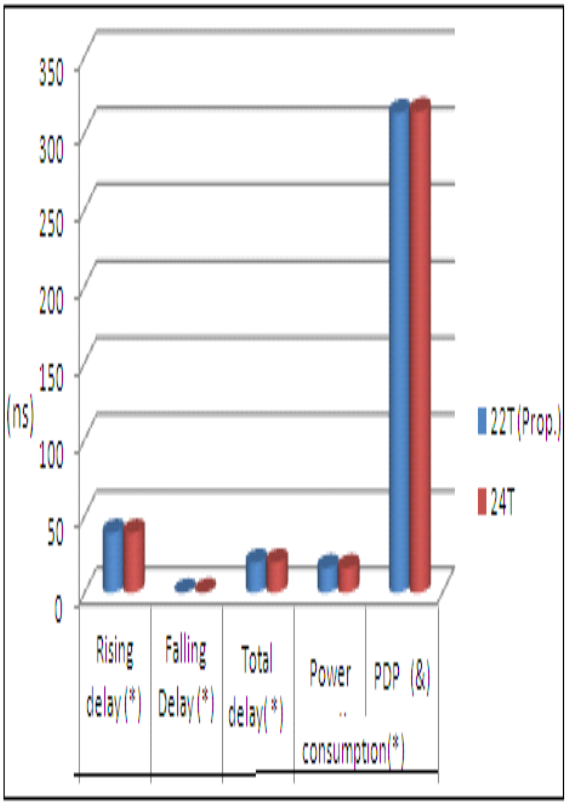


***Fig. 5. Rising delay, propagation delay, power consumption and PDP chart of 1 bit ripple carry adder.***

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## III. EXPERIMENT RESULTS

To describe practical application of the suggested logic circuit 32 bit adder circuit is designed. In 32 bit adder a ripple carry chain of 8 bit is used to give boosting operation at each stage of carry chain. Fig. 6 shows the suggested 8 bit ripple carry chain used in BCDL.

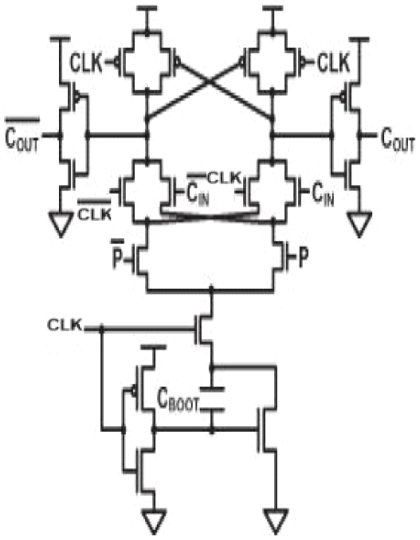


*Fig.6. Proposed 8 bit ripple carry chain in bcdl*

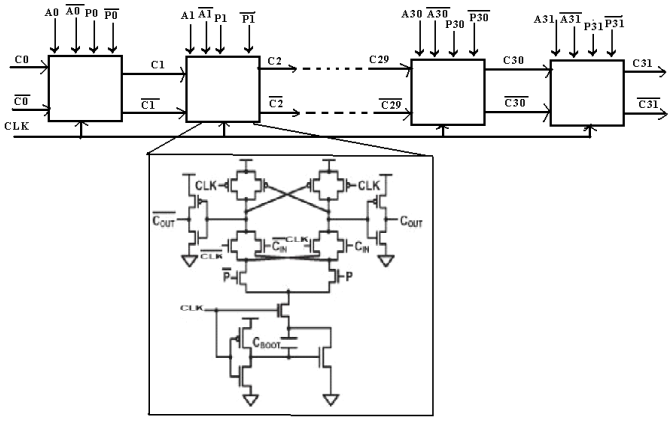


*Fig. 7 . Structure of 1 bit ripple carry chain in 32 bit BCDL adder*

Table 2 shows the total delay, power consumption and power delay product of 32 bit ripple carry adder.

***Table. 2. 32 bit ripple carry adder***

| 32 bit Ripple Carry Adder | Rising delay (*) | Falling Delay (*) | Total delay(*) | Power consumption($) | PDP (&) |
|---|---|---|---|---|---|
| 704T (Prop.) | .39 | .14 | 19.57 | 10 | 195 |
| 768T | .39 | .22 | 19.61 | 10 | 196 |
| Units- *=ns, &=ns x ns $=µm | | | | | |

Fig.8 shows the rising delay, propagation delay, power consumption and PDP chart of 32 bit ripple carry adder.

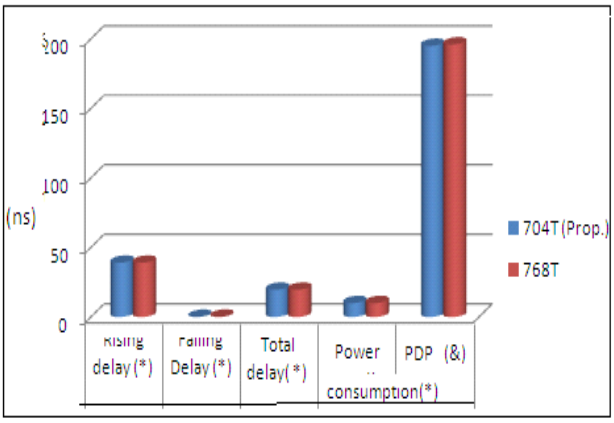


***Fig.8 Rising delay, propagation delay, power consumption and PDP chart of 32 bit ripple carry adder***

The proposed 8 bit ripple carry adder waveform is shown in Fig. 9

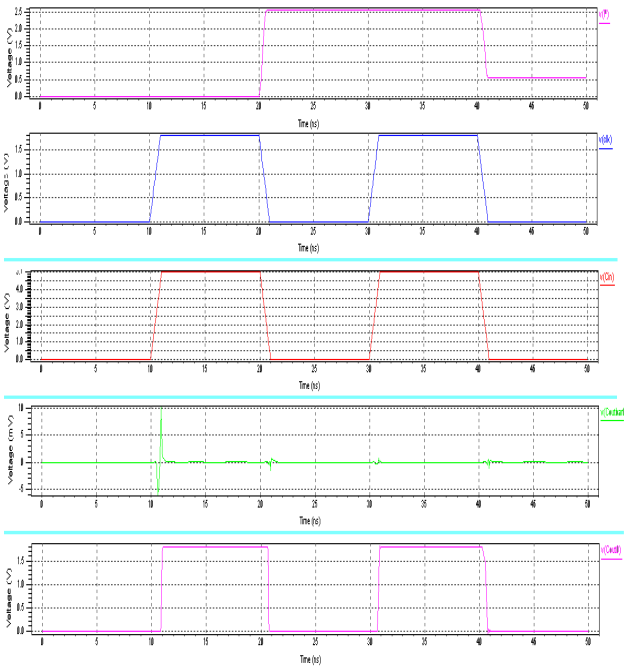

***Fig. 9 Proposed 8 bit ripple carry adder waveform***

***Table 3.Shows the rising delay, propagation delay, power consumption and PDP chart of 64 bit ripple carry adder.***

| 64 bit ripple carry adder | Rising delay(ns) | Falling delay(ns) | Total delay(ns) | Power consumption(um) | PDP(ns) |
|---|---|---|---|---|---|
| 1408(Proposed) | -39 | .14 | 19.57 | 10 | 195 |
| 1536 | -39 | .14 | 19.57 | 10 | 196 |

## IV. CONCLUSION

Boosted CMOS differential logic circuit with feature of voltage boosting has been described. The BCDL gives high switching speed when compared to the previous logic circuits at low supply voltage through a single boosting circuit shared by complementary outputs. The BCDL reduces the area also. Difference results in a tsmc 0.180 um CMOS process shows that product of energy delay given by the suggested logic circuits were improved compared to previous logic circuits. The experiment result for a 64 bit designed with BCDL logic circuits indicate that there is a reduction in the addition time.

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